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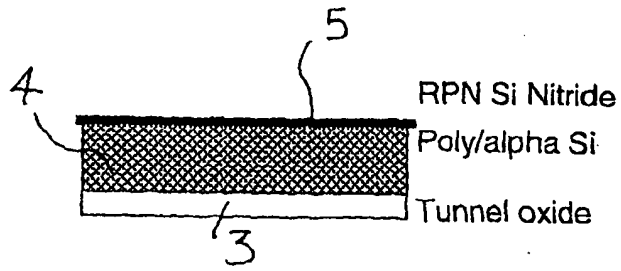
(54) Interpoly dielectric manufacturing process for non volatile semiconductor memories

(57) The invention relates to a process for manufacturing an interpoly dielectric layer (2) for non-volatile memory cells of a semiconductor device with an interpoly dielectric layer (2). The process begins with forming the tunnel oxide (3), and hence the amorphous or polycrystalline silicon layer (4), using conventional techniques. After the amorphous or polycrystalline silicon layer (4) is surface cleansed and passivated, the surface of the polycrystalline layer (4) is :nitrided directly by using radical nitrogen. This is followed by the formation of the interpoly dielectric, either as an ONO layer or a single silicon layer, by means of the CVD technique. Masking to define the floating gate may be performed immediately before or after the direct nitridation step is carried out. The equivalent electrical thickness of the interpoly dielectric, obtained by combining the nitride oxide layer and by the following dielectric, doesn't exceed 130 Angstroms in either the ONO layer or the single silicon layer embodiment.

FIG. 4



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Description

Field of Application

[0001] The present invention relates to the manufacturing of semiconductor memory devices, such as non-volatile memories of the flash EEPROM (Electrically Erasable Programmable Read-Only Memories) type. Flash EEPROM memories can be erased with one operation in all the cells forming the memory.

[0002] More particularly, the invention relates to the manufacturing of a non-volatile memory cell, e.g. of the flash EEPROM type, with a substantially thinner interpoly dielectric than the prior art, yet capable of ensuring proper performance of the device in terms of electrical characteristics and capability to retain a programmed logic state.

[0003] The invention further relates to a process for manufacturing, on a very large integration scale as well as on a single wafer, non-volatile memory devices of the flash EEPROM type having the above-outlined features.

Prior Art

[0004] As it is well known in this particular technical field, re-programmable non-volatile memory cells, in particular flash EEPROM cells, are structured as a floating gate FETs (Field-Effect Transistors) and have a dielectric layer, called the interpoly dielectric, provided between their floating and control gate regions, this dielectric layer functioning as an insulator to the charge stored in the floating gate. The absence or presence of charge in the floating gate effectively sets the logic state of the memory, which logic state is defined as 0 or 1 in the binary code.

[0005] The above dielectric layer is obtained in different ways and made out of different materials. A common procedure is to deposit three dielectric layers successively onto the floating gate region, this region being formed by a layer of amorphous or polycrystalline silicon (polysilicon) deposited onto a thin layer of silicon oxide known as the tunnel oxide. The so obtained multiple dielectric layer comprises: a first layer of silicon oxide, a second layer of silicon nitride, and a third layer of silicon oxide. The resulting dielectric is known as the ONO or ONO interpoly dielectric, as it is shown in Figure 1.

[0006] Within the ONO layer, the cell capability to retain its logic state is mainly guaranteed by two layers of silicon oxide. Indeed, the nitride layer facilitates integration of the triple layer inside the flow of the device manufacturing process. During the manufacturing steps that follow the formation of the interpoly dielectric, treatments made with oxidizing species (O_2, O, OH, H_2O) are applied. The nitride acts as a barrier against the diffusion of the oxidizing species to the floating gate, since it is not permeable to said oxidizing species. Thus, its presence is effective to prevent further oxidation of the floating gate, and therefore, the thickness of the interpoly dielectric from being changed in the course of subsequent steps of the device manufacturing process. In the state of the art, the need to have a nitride layer maintained sufficiently thick to shield from subsequent thermal treatments, and the concurrent need to keep the retention capability of the ONO layer unchanged, disallows to reduce the overall electrical thickness of the triple layer below 140 Angstroms.

[0007] Instead of ONO layer, a single oxide interpoly layer may be used whenever, in specific memory cells, the interpoly dielectric is not required to be particularly thin and/or no oxidizing treatments are provided after its formation. The thickness of the interpoly dielectric is, irrespective of its composition and forming method, jointly responsible of the capacitive coupling of the memory cell. Accordingly, it enters the setting of program and erase parameters, additionally to ensuring retention of the logic state over time.

[0008] A pressing demand for increased miniaturization of electronic devices and reduced power absorption, and the consequent need for ever lower device bias voltages, is urging recourse to active dielectrics of reduced thickness at no trade-off of their performance characteristics.

[0009] It has been proposed, in prior patent specifications to the filing date of this Application, that a layer of silicon nitride be included in the manufacturing of flash memory cells. This layer is used in the ONO triple layer, and used for protection against mechanical and thermal stressing during the intermediate manufacturing steps, but is removed before the manufacturing process is completed. Such are the teachings of US 5,352,619, for instance.

[0010] US Patent 6,137,132 discloses using the silicon nitride as an antireflection material for the subsequent photoetching application. According to US Patent 5,926,730, the silicon nitride is provided at the interface between the bottom silicon layer and a conductive layer within an active dielectric stack.

[0011] The underlying technical problem of this invention is to provide a method of manufacturing flash memory cells, whereby the combined thickness of the dielectric layers between the floating and control gate regions can be reduced at 130 Angstroms or less, thereby improving or maintaining still the cell characteristics. The cell characteristics are: good capacitive coupling of the floating gate to the control gate, small leakage through the active and passive dielectric layers, long-term retention of charge, and reduced power usage by reason of the memory cell components having lower resistivity.

Summary of the Invention

[0012] The present invention is directed to solve the technical problem set in the preceding paragraph by having, interposed between the floating gate and the ONO interpoly dielectric or the dielectric constituted only by silicon oxide, a layer of silicon nitride oxide (oxyni-

tride) which is obtained by direct nitridation of the polysilicon surface in the floating gate region using radical nitrogen.

[0013] By nitriding the polysilicon surface directly, the overall electrical thickness of the interpoly dielectric obtained by the combination of the nitride oxide layer and the following dielectric layer can be brought down to 130 Angstroms or less in the options of ONO layer or the single silicon oxide layer (single oxide interpoly).

[0014] Based on this concept, the technical problem is solved by a process as previously indicated and as defined in Claim 1 and foll..

[0015] The invention further relates to an interpoly dielectric layer structure as defined in Claim 12 and foll..

[0016] The features and advantages of the process and the structure according to the invention will be apparent from the following description of embodiments thereof, given by way of non-limitative examples with reference to the accompanying drawings.

Brief Description of the Drawings

[0017]

Figure 1 shows a photo representation of a conventional flash memory cell obtained by an electron microscope.

Figures 2 to 6 are schematical enlarged vertical cross-section views taken through a portion of a flash memory cell during the process step according to the invention.

Figures 7 and 8 are schematical enlarged vertical cross-section views taken through a portion of a flash memory cell during the process step according to a modified embodiment of the invention.

Detailed Description

[0018] Referring to figures 1 and 2, and particularly to the example shown in Figure 1, a substrate of a semiconductor material, e.g. monocrystalline silicon, is generally shown at 1 in schematic form. This substrate is subjected by a series of process phases as provided by the method of this invention.

[0019] The process phases and the structures described hereinafter do not form a complete process flow for manufacturing integrated circuits. Indeed, the invention can be used in combination with currently used integrated circuits manufacturing techniques, and only such conventional steps as are necessary to an understanding of this invention will be discussed here.

[0020] Drawing views that show cross-sections through portions of an integrated circuit during its manufacturing are not drawn to scale, but rather to highlight important features of the invention.

[0021] The process of forming an interpoly dielectric layer 2 for a non-volatile flash memory cell is carried out according to the steps hereafter described. It should be noted that the step of directly nitriding the amorphous or polycrystalline silicon layer is the same, and is followed by two alternative options, as concerning the dielectric depositing steps.

[0022] A first of these alternative steps is marked "a" hereinafter and consists of depositing ONO interpoly dielectric by the CVD (Chemical Vapor Deposition) technique onto batch or single wafers.

[0023] The second step is marked "b" hereinafter and consists of depositing single oxide interpoly dielectric by the CVD (Chemical Vapor Deposition) technique onto batch or single wafers.

[0024] 1a-b A layer of tunnel oxide 3 is grown over the substrate 1 and followed by the deposition of an amorphous or polycrystalline silicon layer 4, as shown in Figure 1.

[0025] 2a-b This process step may be carried out now, or alternatively as step 5a-b below. This step consists of exposing a mask to define the floating gate region. Masking is followed by dry etching the amorphous or polycrystalline layer and then removing the residual resist from the wafer.

[0026] 3a-b The surface of the amorphous or polycrystalline layer 4 used in forming the floating gate of the device is surface cleansed by means of chemicals in aqueous solution. This treatment is applied by either growing native chemical oxide, or by passivating said surface with Si-H bonds, or by wet or vapor HF-last, subsequent to the aqueous cleansing treatment.

[0027] 4a-b Advantageously in this invention, said surface is nitrided directly using radical nitrogen, on either batch or single wafers. Radical nitrogen (N+) is obtained by subjecting N_2 molecules to a plasma. According to the design of the radical nitrogen generator, this technology, for example, is known as RPN (Remote Plasma Nitridation), DPN (Decoupled Plasma Nitridation), and MRG (Magnetic Radical Generator). The above direct nitriding operation is to grow a thin layer 5 of silicon nitride oxide serving dual functions:

i) improving the interface quality between the floating gate and the interpoly dielectric; and

ii) in those cases where the interpoly dielectric is a single oxide interpoly, preventing oxidizing chemicals, such as O_2, O, OH, and H_2O, from migrating to the floating gate during later treatments subjected to the memory device being formed.

[0028] The nitride oxide layer 5 can be regarded as a barrier layer.

[0029] The silicon nitride oxide layer 5, obtained by direct surface nitridation of layer 4 as explained above and shown in Figure 4, has preferably a thickness dimension of 0.5 to 5.0 nm.

[0030] The nitrogen distribution inside of said layer 5,

as estimated by the SIMS/TOF-SIMS method, should be no less than 1e22 at/cm^3 as peak value, for a total amount of no less than 1e15 at/cm^2. The direct surface nitridation processes using radical nitrogen are carried out at temperatures of 500° to 800°C for 30 seconds (30") to 3 minutes (3') on single wafers. Either N_2 alone or nitrogen/inert gas mixtures such as N_2/He and N_2/Ar may be used as the process gas.

[0031] 5a-b This step is carried out, only when step 2a-b is skipped , using the same procedure as for step 2a-b.

[0032] 6a The interpoly dielectric 2 can now be formed as either an ONO (Oxide-Nitride-Oxide) triple layer, e. g. by using a CVD (Chemical Vapor Deposition) technique onto batch or single wafers. The physical thicknesses of the individual ONO layers are chosen so that the final electrical thickness of the interpoly dielectric is not greater than 130 Å.

[0033] 7a Optionally, the deposited interpoly dielectric may be densified by thermal treatment using O_2, N_2, or H_2O species.

[0034] A modified embodiment of the inventive process will now be described with reference to Figures 7 to 9. This embodiment comprises forming a single dielectric layer 7 on top of the nitride oxide barrier layer 5. The steps described here below are alternative to steps 6a and 7a above.

[0035] 6b The interpoly dielectric 2 is formed using the single oxide interpoly option, on either batch or single wafers. Briefly, a single dielectric layer 7 is deposited onto the barrier layer 5. The physical thickness of layer 7 is chosen so that the final electrical thickness of the dielectric interpoly is not greater than 130 Angstroms.

[0036] 7b Optionally, the deposited single layer 7 may be densified by thermal treatment using O_2, N_2, or H_2O species.

[0037] The direct nitridation of the amorphous or polycrystalline silicon layer using radical nitrogen succeeds in obtaining a very thin layer having a high nitrogen content, which would be impossible to achieve by conventional nitridation techniques.

[0038] By providing a barrier between the floating gate and the interpoly dielectric, the dielectric quality is improved such that the overall thickness of the layer can be reduced to 130 Angstroms or even more. Also, the resistance of said layer to oxidizing species allows an interpoly dielectric to be inserted which comprises a single oxide interpoly layer, and this even in devices for which the process provides subsequent oxidizing treatments.

[0039] Thus, a combination of the nitridation technique with conventional CVD, in order to form the interpoly dielectric in either of the aforementioned options (i. e. ONO interpoly or single oxide interpoly), affords a significant advantage over prior art methods. This advantage is that of the reduction of the overall electrical thickness of the interpoly dielectric, down to 130 Angstroms or less while keeping the charge retention capability of the memory device unchanged.

Claims

1. A process for manufacturing an interpoly dielectric (2) for non-volatile memory cells of a semiconductor device, wherein at least one thin oxide layer (3) is deposited onto a semiconductor substrate (1), and an amorphous or polycrystalline silicon layer is deposited onto said thin oxide layer (3) to form a floating gate region of the memory cell, **characterized by** the step of direct nitriding the surface of said amorphous or polycrystalline silicon layer (4), using radical nitrogen, thereby forming a thin layer (5) of silicon nitride oxide thereon.

2. A process according to Claim 1, **characterized in that** the thickness of the silicon nitride oxide layer (5), formed by direct nitridation, varies between 0.5 to 5.0 nm.

3. A process according to Claim 1, **characterized in that** the nitrogen distribution inside the silicon nitride oxide layer (5), formed by direct nitridation, should be no less than 1e22 at/cm^3 as peak value, for a total amount of no less than 1e15 at/cm^2, as estimated by the SIMS/TOF-SIMS method.

4. A process according to Claim 1, **characterized in that** the interpoly dielectric (2) is formed, on either batch or single wafers systems, subsequently to said direct nitridation step.

5. A process according to Claim 1, **characterized in that** a masking step directed to define the floating gate region of the cell and a step of dry etching the amorphous or polycrystalline silicon layer (4) are carried out immediately before said direct nitridation step.

6. A process according to Claims 1 to 4, **characterized in that** a masking step to define the floating gate region of the cell and a step of dry etching the amorphous or polycrystalline silicon layer (4) are carried out immediately after the direct nitridation step.

7. A process according to Claim 1, **characterized in that** above said nitride oxide layer (5) is provided the formation of the interpoly dielectric (2), comprising a triple ONO layer (6) and by means of the CVD.

8. A process according to Claim 7, **characterized in that** the overall electrical thickness of the interpoly dielectric, obtained by combining the nitride oxide layer (5) and the ONO triple layer (6), is equal to or less than 130 Angstroms.

9. A process according to Claim 1, **characterized in that** above said nitride oxide layer (5) is provided the formation of the interpoly dielectric (2), comprising a single layer (7) of silicon oxide and by means of the CVD.

10. A process according to Claim 9, **characterized in that** the overall electrical thickness of the interpoly dielectric obtained by combining the nitride oxide layer (5) and the single silicon oxide layer (7) is equal to or less than 130 Angstroms.

11. A process according to Claim 7, **characterized in that** said ONO interpoly triple layer (6) is densified by heat treatment under an N_2, H_2O and O_2 atmosphere.

12. A process according to Claim 9, **characterized in that** said single-ply interpoly (7) is densified by heat treatment under an N_2, H_2O and O_2 atmosphere.

13. An interpoly dielectric structure for non-volatile memories comprising memory cells with floating gate transistors, wherein said dielectric layer separates a floating gate region from a control gate region, **characterized in that** it comprises a thin layer (5) of silicon nitride oxide formed above the floating gate region, said thin layer (5) formed according to the process of Claim 1.

FIG. 1

Interpoly Dielectric
Flash memory Application
Interpoly dielectric

FIG. 2

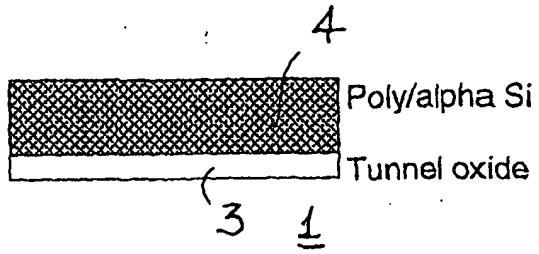


FIG. 3

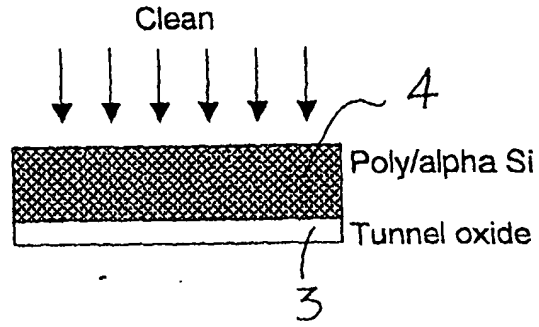


FIG. 4

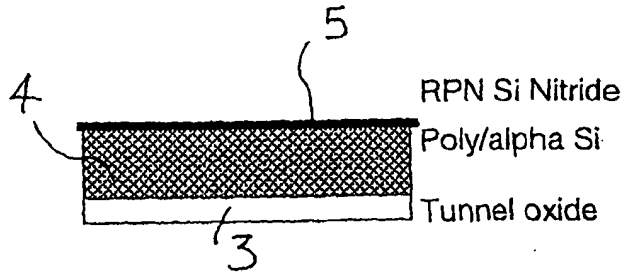


FIG. 5

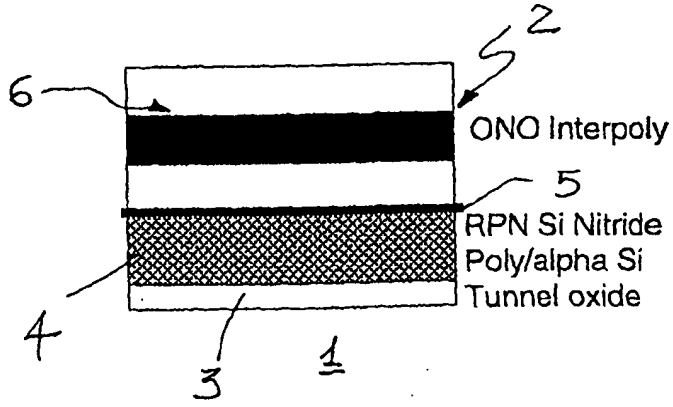


FIG. 6

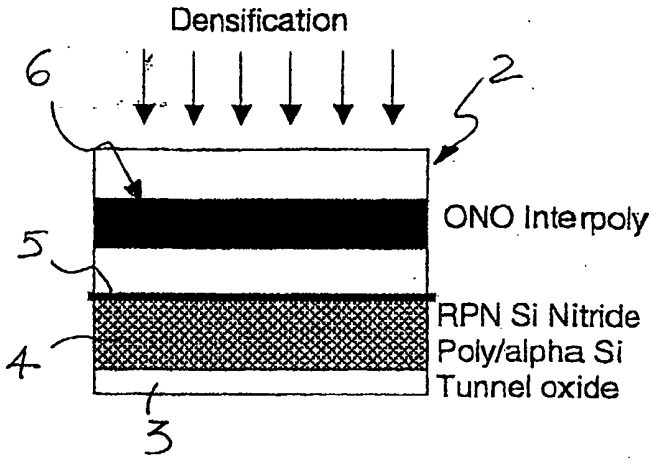


FIG. 7

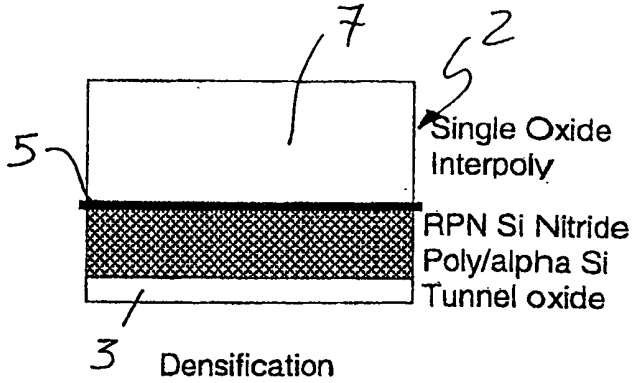
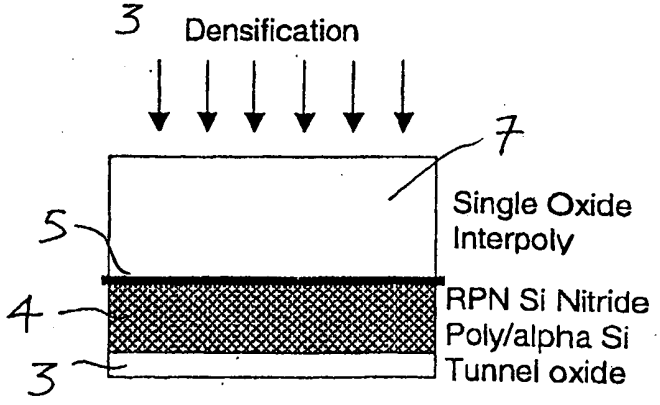


FIG. 8



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EUROPEAN SEARCH REPORT

Application Number
EP 02 42 5044

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 6 127 227 A (CHEN JONG ET AL) 3 October 2000 (2000-10-03)	1-10,13	H01L21/28 H01L29/788
Y	* the whole document *	11,12	
Y	US 6 162 684 A (CHANG KENT KUOHUA ET AL) 19 December 2000 (2000-12-19)	11,12	
A	* the whole document *	1,7-10	
X	US 5 888 870 A (GILMER MARK C ET AL) 30 March 1999 (1999-03-30)	1,4-6,13	
A	* column 6, line 12 - column 8, line 4; figures 2-12 *	2,7-12	
A	US 5 557 122 A (REDDY CHITRANJAN N ET AL) 17 September 1996 (1996-09-17) * column 4, line 35 - column 6, line 65; figures 2-4 *	1-13	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	4 July 2002	Albrecht, C

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04-07-2002

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